

WHAT IS CLAIMED IS:

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1. A display device comprising:

a pixel portion in which  $(m \times 2n)$  pixels, each including at least one TFT, are arranged in matrix form (both  $m$  and  $n$  are natural numbers);

5 a source driver for supplying video signals to  $2n$  source signal lines  $S1, S2, \dots, Sn, Sn+1, Sn+2, \dots, S2n$ ;

a first gate driver for supplying selection signals to  $m$  first gate signal lines  $G1L, G2L, \dots, GmL$ ; and

10 a second gate driver for supplying selection signals to  $m$  second gate signal lines  $G1R, G2R, \dots, GmR$ , wherein:

the pixels connected to the source signal lines  $S1, S2, \dots, Sn$  are supplied with the selection signals from the first gate signal lines  $G1L, G2L, \dots, GmL$ ;

the pixels connected to the source signal lines  $Sn+1, Sn+2, \dots, S2n$  are supplied with the selection signals from the second gate signal lines  $G1R, G2R, \dots, GmR$ ;

the selection signal starts to be supplied to the second gate signal line  $G1R$  while the selection signal is supplied to the first gate signal line  $G1L$ ; and

the selection signal starts to be supplied to the first gate signal line  $G1L$  while the selection signal is supplied to the second gate signal line  $G1R$ .

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2. A display device comprising:

a pixel portion in which  $(m \times 2n)$  pixels, each including at least one TFT, are arranged in matrix form (both  $m$  and  $n$  are natural numbers);

a source driver for supplying video signals to  $2n$  source signal lines  $S1, S2, \dots, Sn, Sn+1, Sn+2, \dots, S2n$ ;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ..., GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ..., GmR, wherein:

5 the pixels connected to the source signal lines S1, S2, ..., Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, ..., GmL;

the pixels connected to the source signal lines Sn+1, Sn+2, ..., S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, ..., GmR; and

the selection signals are sequentially supplied to the first gate signal line G1L, the second gate signal line G1R, the first gate signal line G2L, the second gate signal line G2R, ..., the first gate signal line GmL, and the second gate signal line GmR in this order with a delay of a half period between the respective adjacent gate signal lines.

3. A rear projector comprising three display devices according to claim 1.

4. A rear projector comprising three display devices according to claim 2.

5. A front projector comprising three display devices according to claim 1.

20 6. A front projector comprising three display devices according to claim 2.

7. A rear projector comprising one display device according to claim 1.

8. A rear projector comprising one display device according to claim 2.

9. A front projector comprising one display device according to claim 1.
10. A front projector comprising one display device according to claim 2.
- 5 11. A head mount display comprising a display device according to claim 1.
12. A head mount display comprising a display device according to claim 2.
13. A Computer comprising a display device according to claim 1.
- 10 14. A Computer comprising a display device according to claim 2.
15. A video camera comprising a display device according to claim 1.
16. A video camera comprising a display device according to claim 2.
17. A DVD player comprising a display device according to claim 1.
18. A DVD player comprising a display device according to claim 2.
- 20 19. A display device comprising a display device according to claim 1.
20. A display device comprising a display device according to claim 2.

21. A display device according to claim 1 is a liquid crystal display device.

22. A display device according to claim 2 is a liquid crystal display device.

Sub C3  
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23. A method of driving an active matrix display device comprising:  
a pixel portion in which  $(m \times 2n)$  pixels, each including at least one TFT, are arranged in matrix form (both  $m$  and  $n$  are natural numbers);  
a source driver for supplying video signals to  $2n$  source signal lines  $S_1, S_2, \dots, S_n, S_{n+1}, S_{n+2}, \dots, S_{2n}$ ;  
a first gate driver for supplying selection signals to  $m$  first gate signal lines  $G_{1L}, G_{2L}, \dots, G_{mL}$ ; and  
a second gate driver for supplying selection signals to  $m$  second gate signal lines  $G_{1R}, G_{2R}, \dots, G_{mR}$ , wherein said method comprises the steps of:  
supplying the pixels connected to the source signal lines  $S_1, S_2, \dots, S_n$  with the selection signals from the first gate signal lines  $G_{1L}, G_{2L}, \dots, G_{mL}$ ;  
supplying the pixels connected to the source signal lines  $S_{n+1}, S_{n+2}, \dots, S_{2n}$  with the selection signals from the second gate signal lines  $G_{1R}, G_{2R}, \dots, G_{mR}$ ;  
starting to supply the selection signal to the second gate signal line  $G_{1R}$  while the selection signal is supplied to the first gate signal line  $G_{1L}$ ; and  
20 starting to supply the selection signal to the first gate signal line  $G_{1L}$  while the section signal is supplied to the second gate signal line  $G_{1R}$ .

Sub C3  
24. A method of driving an active matrix display device comprising:

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a pixel portion in which ( $m \times 2n$ ) pixels, each including at least one TFT, are arranged in matrix form (both  $m$  and  $n$  are natural numbers);

a source driver for supplying video signals to  $2n$  source signal lines  $S_1, S_2, \dots, S_n, S_{n+1}, S_{n+2}, \dots, S_{2n}$ ;

5 a first gate driver for supplying selection signals to  $m$  first gate signal lines  $G_{1L}, G_{2L}, \dots, G_{mL}$ ; and

a second gate driver for supplying selection signals to  $m$  second gate signal lines  $G_{1R}, G_{2R}, \dots, G_{mR}$ , wherein said method comprises the steps of:

supplying the pixels connected to the source signal lines  $S_1, S_2, \dots, S_n$  with the selection signals from the first gate lines  $G_{1L}, G_{2L}, \dots, G_{mL}$ ;

supplying the pixels connected to the source signal lines  $S_{n+1}, S_{n+2}, \dots, S_{2n}$  with the selection signals from the second gate lines  $G_{1R}, G_{2R}, \dots, G_{mR}$ ;

starting to supply the selection signal to the second gate signal line  $G_{1R}$  while the selection signal is supplied to the first gate signal line  $G_{1L}$ ; and

starting to supply the selection signal to the first gate signal line  $G_{1L}$  while the selection signal is supplied to the second gate signal line  $G_{1R}$ .

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